**NAME: Tanmay Karmarkar ROLL NO: 21143**

**CLASS : S.E. COMP SUBJECT : DEL**

**EXPT. NO. : 10 DATE : 15/12/2021**

**TITLE : SEQUENCE DETECTOR CIRCUIT**

**OBJECTIVE :**

**1. To** design and Implement Sequence detector for sequence 101 using JK flip-flop.

**2. To** design and Implement Sequence detector for sequence 110 using JK flip-flop.

**APPARATUS :**

Digital-Board, GP-4 Patch-Cords, IC-74LS76, IC-74LS32, IC-74LS04/IC-74LS08 and Required Logic gates if any

**THEORY :**

1. The sequence detector is a synchronous FSM to detect a sequence applied to the input.

2. It checks the input sequence bit by bit and moves to the next stage if desired bit is obtained.

3. The output of the circuit is zero as long as complete sequence is not detected.

4. The output becomes one as soon as the complete sequence is detected at the input side.

5. It can be implemented by using JK flip-flops.

6. Moore or Mealy model can be used for implementation.

7. Sequence detector for sequence 1-0-1(Moore Model).

**PIN Diagram :**

PRESET1

PRESET2

CLOCK1

CLEAR1

CLEAR2

1

K

J

2

1

Q

1

Q

GND

K

2

Q

2

Q

2

CLOCK2

J

1

VCC

7

4

LS

7

6

D

U

A

L

MS

J-K

FF

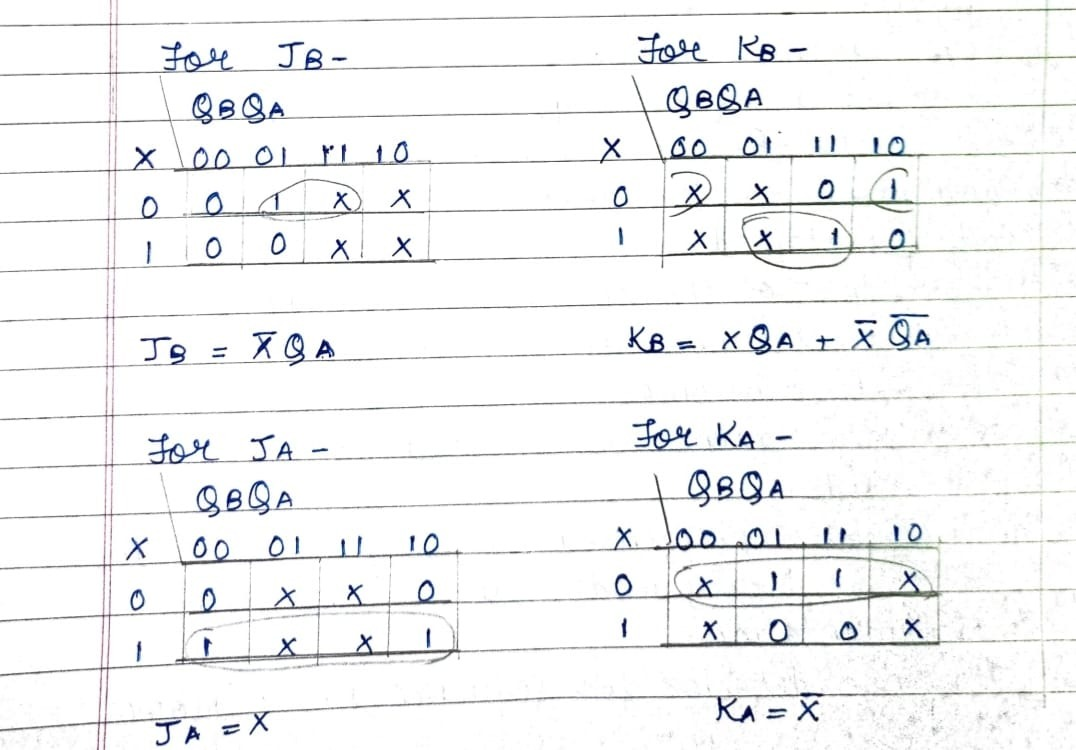
**PROCEDURE :**

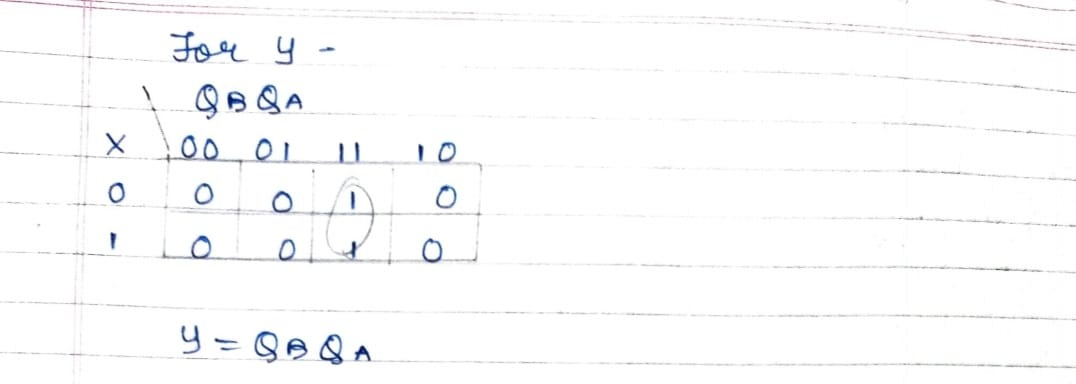
1. Make the connections as per the Logic circuit of Sequence detector circuit using IC74LS76 and Verify its Truth Table.

**Truth Table:**

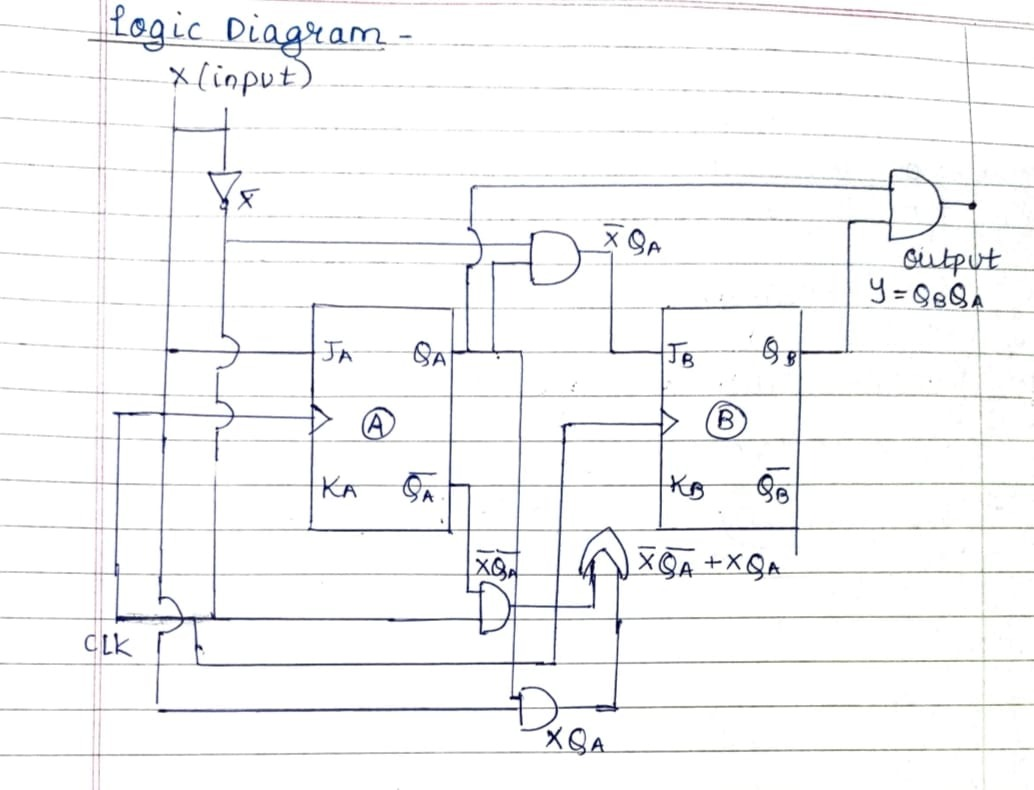
|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUT** | **PRESENT STATE** | | **NEXT STATE** | | **FLIP FLOP INPUTS** | | | | **OUTPUT** |
| **X** | **Qb** | **Qa** | **Qb+** | **Qa+** | **Jb** | **Kb** | **Ja** | **Ka** | **Y** |
| **0** | **0** | **0** | **0** | **0** | **0** | **X** | **0** | **X** | **0** |
| **0** | **0** | **1** | **1** | **0** | **1** | **X** | **X** | **1** | **0** |
| **0** | **1** | **0** | **0** | **0** | **X** | **1** | **0** | **X** | **0** |
| **0** | **1** | **1** | **1** | **0** | **X** | **0** | **X** | **1** | **1** |
| **1** | **0** | **0** | **0** | **1** | **0** | **X** | **1** | **X** | **0** |
| **1** | **0** | **1** | **1** | **1** | **0** | **X** | **X** | **0** | **0** |
| **1** | **1** | **0** | **0** | **1** | **X** | **0** | **1** | **X** | **0** |
| **1** | **1** | **1** | **1** | **1** | **X** | **1** | **X** | **0** | **1** |

# K-Map Simplification for JA , KA , JB , KB , JC , KC



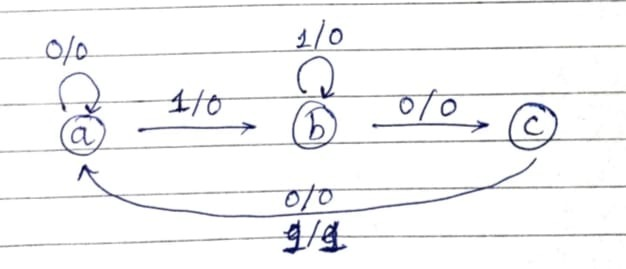


**Logic diagram:**



**Sequence Detector of sequence 101 (Mealy Model)**

**State Diagram:**



**State Table:**

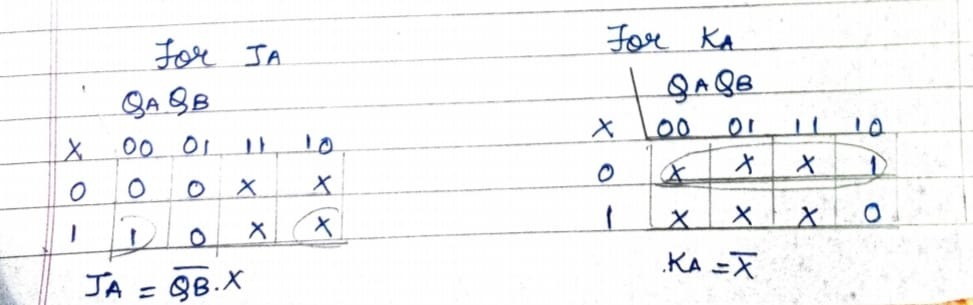
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Present state** | **Next state** | | **Output** | |
| **X=0** | **X=1** | **X=0** | **X=1** |
| **a** | **a** | **b** | **0** | **0** |
| **b** | **c** | **b** | **0** | **0** |
| **c** | **a** | **a** | **0** | **1** |

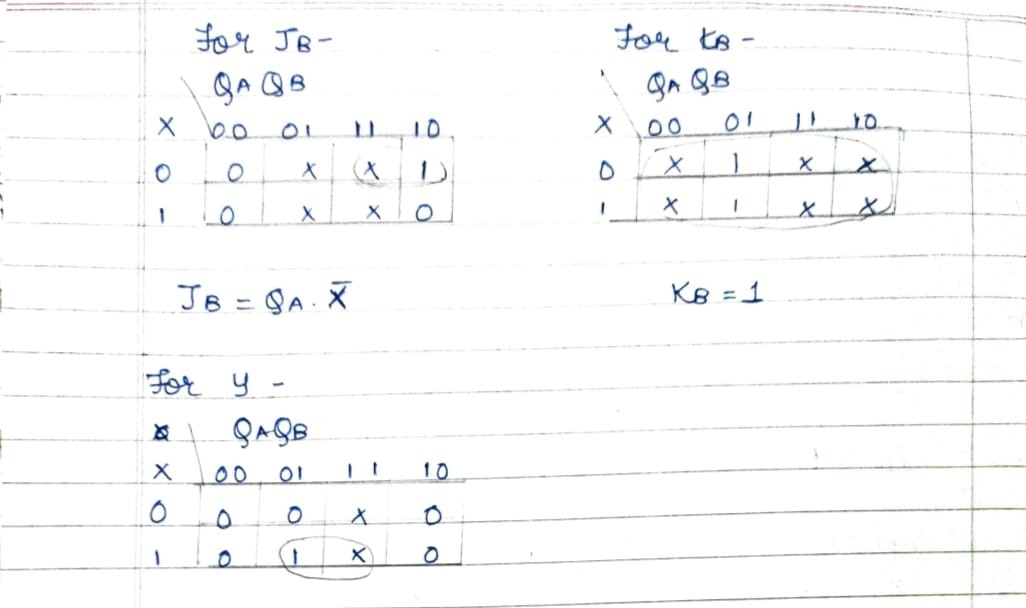
**Where a=00, b=01, c=10 and d=11**

**Circuit Excitation Table:**

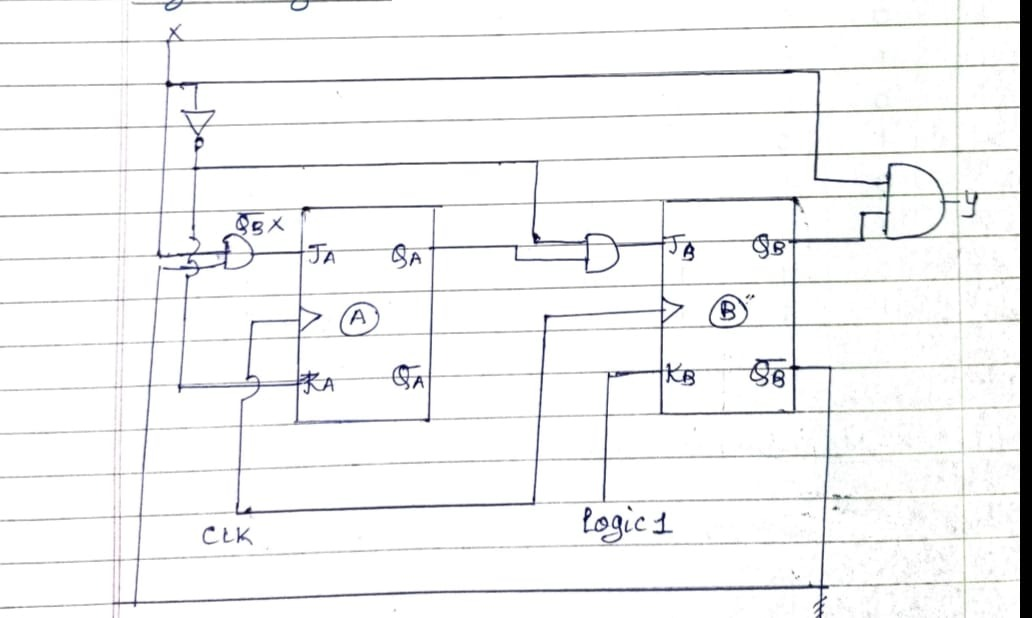
|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUT** | **PRESENT STATE** | | **NEXT STATE** | | **FLIP FLOP INPUTS** | | | | **OUTPUT** |
| **X** | **Qa** | **Qb** | **Qa+** | **Qb+** | **Ja** | **Ka** | **Jb** | **Kb** | **Y** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **X** | **0** |
| **1** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **X** | **0** |
| **0** | **0** | **1** | **0** | **0** | **0** | **X** | **X** | **1** | **0** |
| **1** | **0** | **1** | **0** | **0** | **0** | **X** | **X** | **1** | **1** |
| **0** | **1** | **0** | **0** | **1** | **X** | **1** | **1** | **X** | **0** |
| **1** | **1** | **0** | **1** | **0** | **X** | **0** | **0** | **X** | **0** |
| **0** | **1** | **1** | **X** | **X** | **X** | **X** | **X** | **X** | **X** |
| **1** | **1** | **1** | **X** | **X** | **X** | **X** | **X** | **X** | **X** |

**K-Map simplification:**



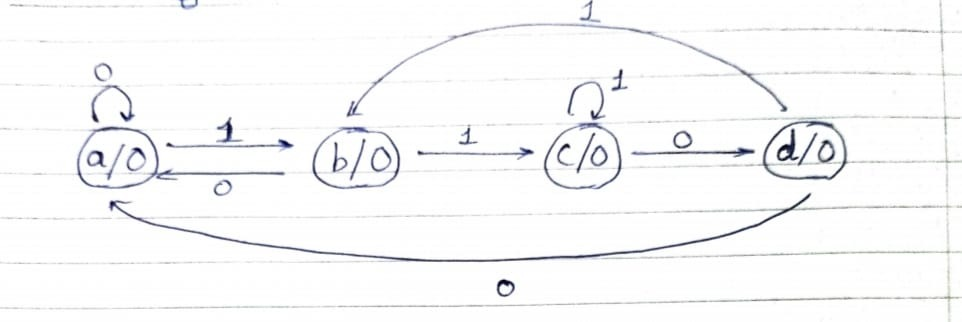


**Logic Diagram:**



**Sequence Detector of sequence 110 (Moore Model)**

**State Diagram:**



**State Table:**

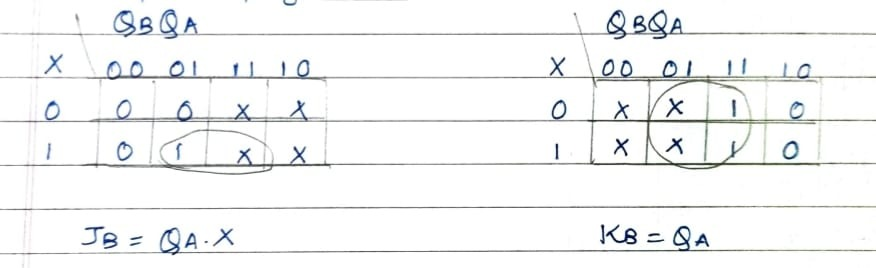
|  |  |  |  |
| --- | --- | --- | --- |
| **Present state** | **Next state** | | **Output** |
| **X=0** | **X=1** | **Y** |
| **a** | **a** | **b** | **0** |
| **b** | **a** | **c** | **0** |
| **c** | **d** | **c** | **0** |
| **d** | **a** | **b** | **1** |

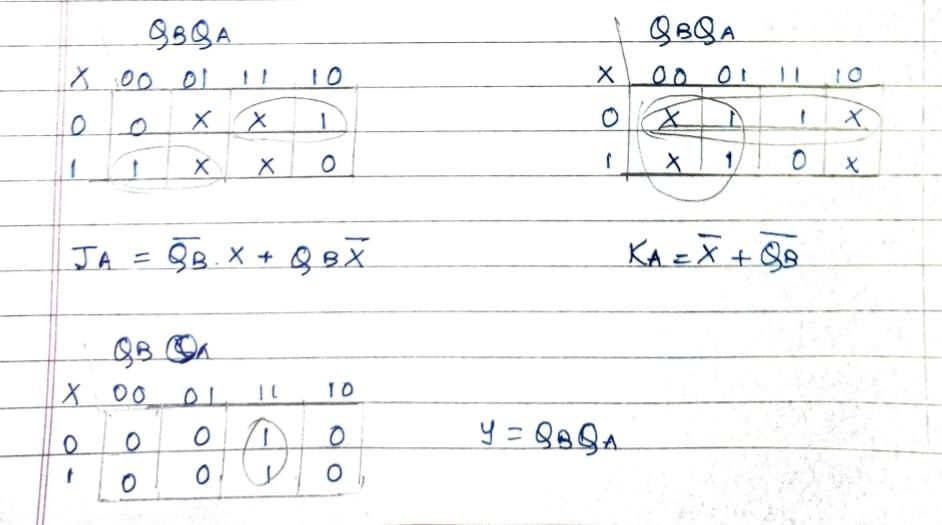
**Where a=00, b=01, c=10 and d=11**

**Circuit Excitation Table:**

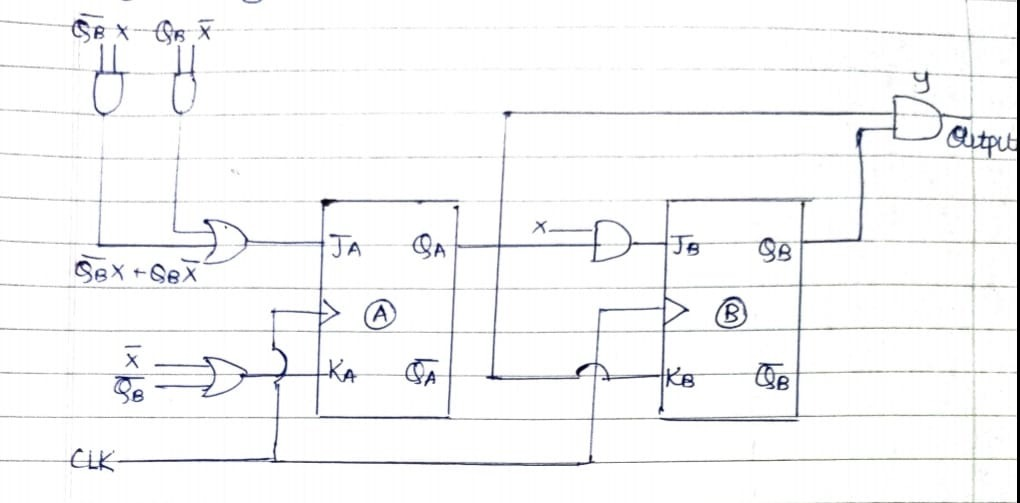
|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUT** | **PRESENT STATE** | | **NEXT STATE** | | **FLIP FLOP INPUTS** | | | | **OUTPUT** |
| **X** | **Qb** | **Qa** | **Qb+** | **Qa+** | **Jb** | **Kb** | **Ja** | **Ka** | **Y** |
| **0** | **0** | **0** | **0** | **0** | **0** | **X** | **0** | **X** | **0** |
| **0** | **0** | **1** | **0** | **0** | **0** | **X** | **X** | **1** | **0** |
| **0** | **1** | **0** | **1** | **1** | **X** | **0** | **1** | **X** | **0** |
| **0** | **1** | **1** | **0** | **0** | **X** | **1** | **X** | **1** | **1** |
| **1** | **0** | **0** | **0** | **1** | **0** | **X** | **1** | **X** | **0** |
| **1** | **0** | **1** | **1** | **0** | **1** | **X** | **X** | **1** | **0** |
| **1** | **1** | **0** | **1** | **0** | **X** | **0** | **0** | **X** | **0** |
| **1** | **1** | **1** | **0** | **1** | **X** | **1** | **X** | **0** | **1** |

**K-Map simplification:**





**Logic Diagram:**



**Logic Gates / MSI Device required for Implementation:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Sr.No.** | **Title** | **Name of the IC** | **IC Required** |
| 01 | Sequence Detector (101) Mealy Model | JK-FF(IC7476)  NOT(IC 7404)  AND(IC 7408)  OR(IC 7432) | 1  1  1  1 |
| 02 | Sequence Detector (110) Moore’s Model | JK-FF(IC7476)  NOT(IC 7404)  AND(IC 7408)  OR(IC 7432) | 1  1  1  1 |

**CONCLUSION:**

Hence, we have successfully implemented sequence detectors using both Moore’s and Mealy’s Model.

**REFFRENCE:**

1. **R.P.Jain “Modern Digital Electronics” TMH 4th Edition**

1. **D.Leach,Malvino,Saha,”Digital Principles and Applications”,TMH**

Subject teacher Sign with Date Remark